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## » Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

 1. Design of a wideband transmit delta-sigma DAC

Neitola, M.; Kivi, A.; Rahkonen, T.;

Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE Internatio

n

Volume 2, 2-5 Sept. 2001 Page(s):1053 - 1056 vol.2

Digital Object Identifier 10.1109/ICECS.2001.957668

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- 1. **Convergence properties of optimal adaptive carrier phase jitter predictor: jitter**  
Sugar, G.L.; Tretter, S.A.;  
Communications, IEEE Transactions on  
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**IEEE CNF** IEEE Conference Proceeding

- 2. **A new multicarrier transceiver based on the discrete cosine transform**  
Al-Dhahir, N.; Hlaing Minn;  
Wireless Communications and Networking Conference, 2005 IEEE  
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- 3. **OFDM for high bit rate data transmission over measured indoor radio channel**  
Nobles, P.; Halsall, F.;  
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Schniter, P.; Liu, H.;  
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23. **8 GHz, 20mW, fast locking, fractional-N frequency synthesizer with optimum order, 3/5-bit IIR and 3/sup rd/ order 3-bit-FIR noise shapers in 90nm CMOS**  
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[AbstractPlus](#) | Full Text: [PDF\(288 KB\)](#) IEEE CNF

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**1 A methodology for efficient high-level dataflow simulation of mixed-signal front-ends of digital telecom transceivers** 

Gerd Vandersteen, Piet Wambacq, Yves Rolain, Petr Dobrovolný, Stéphane Donnay, Marc Engels, Ivo Bolsens

June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

Full text available:  pdf(241.33 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The explosion of the telecommunications market requires miniaturization and cost-effective realization of the front-ends of transceivers for digital telecommunications. New architectures must therefore be simulated at high level. Current methodologies and corresponding tools suffer from common drawbacks, such as lower accuracy, slow simulation speed, etc. A new methodology has been developed for the efficient simulation, at the architectural level, of mixed-signal front-ends of digital tel ...

**2 Listening to FM radio in software, step by step** 

Eric Blossom

September 2004 **Linux Journal**, Volume 2004 Issue 125

Publisher: Specialized Systems Consultants, Inc.

Full text available:  html(18.64 KB) Additional Information: [full citation](#), [abstract](#)

Software radio is a really big important technology. Don't take our word for it—try this simple project.

**3 CAD methods and synthesis: Task scheduling for power optimisation of multi frequency synchronous data flow graphs** 

Bastian Knerr, Martin Holzer, Markus Rupp

September 2005 **Proceedings of the 18th annual symposium on Integrated circuits and system design SBCCI '05**

Publisher: ACM Press

Full text available:  pdf(262.92 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

During recent years power optimisation has become one of the most challenging design goals in modern communication systems, particularly in the wireless domain. Many different approaches for task scheduling on single or multi-core systems exist, mostly addressing the minimisation of execution time or the number of processors used. The minimisation of the processor's clock frequency by adjusting the supply voltage or directly

by frequency scaling according to the chosen task scheduling has shown ...

**Keywords:** frequency scaling, multi frequency systems, power optimisation, synchronous data flow graphs, task scheduling

#### 4 Signal processing in SETI



D. K. Cullers, Ivan R. Linscott, Bernard M. Oliver

November 1985 **Communications of the ACM**, Volume 28 Issue 11

**Publisher:** ACM Press

Full text available: pdf(3.96 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

The Search for Extraterrestrial Intelligence (SETI), now being planned at NASA, will require a prodigious amount of highly concurrent signal processing to be done in real time by special-purpose hardware.

#### 5 CAD for RF circuits

P. Wambacq, G. Vandersteen, J. Phillips, J. Roychowdhury, W. Eberle, B. Yang, D. Long, A. Demir

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

**Publisher:** IEEE Press

Full text available: pdf(396.98 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

#### 6 GNU radio: tools for exploring the radio frequency spectrum

Eric Blossom

June 2004 **Linux Journal**, Volume 2004 Issue 122

**Publisher:** Specialized Systems Consultants, Inc.

Full text available: html(23.76 KB) Additional Information: [full citation](#), [abstract](#)

Listen to ham, shortwave, AM and FM, and even watchHDTV and invent new communications modes, all on the same hardware.

#### 7 Design Space Exploration for a Wireless Protocol on a Reconfigurable Platform

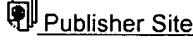
Laura Vanzago, Bishnupriya Bhattacharya, Joel Cambonie, Luciano Lavagno

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

**Publisher:** IEEE Computer Society

Full text available: pdf(175.69 KB)

Additional Information: [full citation](#), [abstract](#), [index terms](#)



This paper describes a design space exploration experiment for a real application from the embedded networking domain & the physical layer of a wireless protocol. The application models both control oriented as well as data processing functions, and hence require composing tasks from different models of computation. We show how the cost and performance of communication and computation can be quickly evaluated, with a reasonable modeling cost. While the example uses a specific tool, the methodology ...

#### 8 Design and Analysis of a Programmable Single-Chip Architecture for DVB-T Base-Band Receiver

Chengzhi Pan, Nader Bagherzadeh, Amir Hosein Kamalizad, Arezou Koohi

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

**Publisher:** IEEE Computer Society

Full text available: [pdf\(342.20 KB\)](#) Additional Information: [full citation](#), [abstract](#), [index terms](#)

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This work treats the design and analysis of a programmable (or reconfigurable) DSP-domain-specific architecture called MorphoSys, upon which world's first single-chip software solution for DVB-T base-band receiver can be implemented. Based on the first version of MorphoSys, many modifications have been made to improve greatly both computation power and data movement efficiency. Sequential codes and SIMD codes can be parallelized; temporal granularity adjustment boosts up performance up to 4 time ...

**9 Area-efficient and reusable VLSI architecture of decision feedback equalizer for QAM** 



Hyeongseok Yu, Byung Wook Kim, Yeon Gon Cho, Jun-Dong Cho, Jea Woo Kim, Hyun Cheol Park, Ki Won Lee

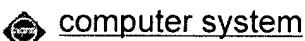
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: [pdf\(176.90 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper, an area efficient VLSI architecture of decision feedback equalizer is derived accommodating 64/256 QAM modulators. This architecture is implemented efficiently in reusable VLSI structure using EDA tool due to its regular structure. The main idea is to employ a time-multiplexed design scheme grouping the adjacent filter taps with correlated internal dataflow and with data transfer having same processing sequence between blocks. We simulated the proposed design scheme using SYN ...

**10 Implementing a RAKE receiver for wireless communications on an FPGA-based** 



Ali M. Shankiti, Miriam Leeser

February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**

Publisher: ACM Press

Full text available: [pdf\(786.81 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

RAKE receivers are widely used in the wireless communications industry. Currently, custom VLSI is the most popular implementation. Programmable and reconfigurable logic implementations are becoming more attractive because of their flexibility and due to technology advancements. We have implemented a RAKE receiver on an Annapolis Wildforce board with four Xilinx 4000 family chips for a total of 100,000 gate equivalents. Our system is able to implement a RAKE receiver for underwater data comm ...

**Keywords:** FPGA, RAKE receiver, wireless communications

**11 An innovative simulation tool for advanced signal processing in UMTS systems** 

Dania Marabissi, Marco Michelini, Luca Simone Ronga

September 2004 **Wireless Networks**, Volume 10 Issue 5

Publisher: Kluwer Academic Publishers

Full text available: [pdf\(545.12 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Link-level simulations are essential in the design of UMTS communication systems. The large number of interdependent variables makes it impossible to derive easy design steps without an efficient modeling of the environments and the implemented reception schemes. In this paper, a novel tool for UMTS design is presented. The tool includes a fast C++ simulation engine and a complete 3GPP library to model the uplink transmission chain. As an example, a series of Monte Carlo performance simulatio ...

**Keywords:** 3G-simulation environment, CDMA advanced receivers, DSP system design, code division multiple access (CDMA), fading channel models, multirate systems, object-oriented simulation tool

**12 Case studies: A case study of mapping a software-defined radio (SDR) application on a reconfigurable DSP core**

Behzad Mohebbi, Eliseu Chavez Filho, Rafael Maestre, Mark Davies, Fadi J. Kurdahi  
October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

**Publisher:** ACM Press

Full text available:  [pdf\(446.86 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

We present a case study involving the implementation of a complete Wideband CDMA (WCDMA) digital receiver part of an AMR channel onto a reconfigurable core. WCDMA is one of the two major standards for the third generation (3G) cellular systems.

Traditionally most of the receiver components were confined to ASIC implementation for performance, size and power consumption reasons. The MS1 reconfigurable DSP core provides both a microprocessor and reconfigurable fabric as well as a variety of periph ...

**Keywords:** reconfigurable computing, software-defined radio

**13 Low power DSP's for wireless communications (embedded tutorial session)**

Ingrid Verbauwhede, Chris Nicol  
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

**Publisher:** ACM Press

Full text available:  [pdf\(424.32 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Wireless communications and more specifically, the fast growing penetration of cellular phones and cellular infrastructure are the major drivers for the development of new programmable Digital Signal Processors (DSPs). In this tutorial, an overview will be given of recent developments in DSP processor architectures, that makes them well suited to execute computationally intensive algorithms typically found in communications systems. DSP processors have adapted instruction sets, memory archi ...

**Keywords:** architectures, digital signal processing, programmable processors, wireless communications

**14 Thermal Modeling, Characterization and Management of On-Chip Networks**

Li Shang, Li-Shiuan Peh, Amit Kumar, Niraj K. Jha  
December 2004 **Proceedings of the 37th annual IEEE/ACM International Symposium on Microarchitecture MICRO 37**

**Publisher:** IEEE Computer Society

Full text available:  [pdf\(551.38 KB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#)

Due to the wire delay constraints in deep submicron technology and increasing demand for on-chip bandwidth, networks are becoming the pervasive interconnect fabric to connect processing elements on chip. With ever-increasing power density and cooling costs, the thermal impact of on-chip networks needs to be urgently addressed. In this work, we first characterize the thermal profile of the MIT Raw chip. Our study shows networks having comparable thermal impact as the processing elements and contr ...

**15 Fault-Tolerant Techniques for Ambient Intelligent Distributed Systems**

Diana Marculescu, Nicholas H. Zamora, Phillip Stanley-Marbell, Radu Marculescu  
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

**Publisher:** IEEE Computer Society

Full text available:  pdf(466.94 KB) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Ambient Intelligent Systems provide an unexplored hardware platform for executing distributed applications under strict energy constraints. These systems must respond quickly to changes in user behavior or environmental conditions and must provide high availability and fault-tolerance under given quality constraints. These systems will necessitate fault-tolerance to be built into applications. One way to provide such fault-tolerance is to employ the use of redundancy. Hundreds of computational devices ...

**16 Getting to the bottom of deep submicron** 

 Dennis Sylvester, Kurt Keutzer

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

**Publisher:** ACM Press

Full text available:  pdf(1.22 MB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

**Keywords:** ASIC, CMOS scaling, gate delay, interconnect modeling, power dissipation, signal integrity, wirelength

**17 Digital Computer System for Dynamic Analysis of Speech and Sound Feedback** 

 **Mechanisms**

K. U. Smith, S. D. Ansell, J. Koehler, G. H. Servos

April 1964 **Journal of the ACM (JACM)**, Volume 11 Issue 2

**Publisher:** ACM Press

Full text available:  pdf(1.03 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The aim of the research reported is to put the laboratory application of closed-loop digital computer systems to experimental control and analysis in biology and behavioral science on a formal basis, using special concepts of programming to quantitatively control different parameters of variation in sensory feedback of specific response systems. The theory is unconventional in that the computer and the techniques of closed-loop programming are designed to control time delays, space displacements ...

**18 Getting around the task-artifact cycle: how to make claims and design by scenario** 

 John M. Carroll, Mary Beth Rosson

April 1992 **ACM Transactions on Information Systems (TOIS)**, Volume 10 Issue 2

**Publisher:** ACM Press

Full text available:  pdf(2.41 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We are developing an "action science" approach to human-computer interaction (HCI), seeking to better integrate activities directed at understanding with those directed at design. The approach leverages development practices of current HCI with methods and concepts to support a shift toward using broad and explicit design rationale to reify where we are in a design process, why we are there, and to guide reasoning about where we might go from there. We represent a designed artifact ...

**Keywords:** design rationale, planning, user interfaces

**19 An integrated temporal partitioning and partial reconfiguration technique for design****latency improvement**

Satish Ganesan, Ranga Vemuri

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: ACM Press

Full text available:  [pdf\(90.90 KB\)](#) [Publisher Site](#)Additional Information: [full citation](#), [references](#), [index terms](#)**20 Approximations for simulation run-time reduction**

G. M. Herman

December 1968 **Proceedings of the second conference on Applications of simulations**

Publisher: Winter Simulation Conference

Full text available:  [pdf\(667.39 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The age of more complex computing systems has made it increasingly important to have reliable means of evaluating the performance of existing systems, and of future systems during their design and development. This latter aspect is only beginning to come into being, and shows great promise of yielding large benefits to the industry. Where most evaluation was, and still is, applied to the evaluation of existing systems for various applications, it is becoming increasingly recognized as a val ...

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L5	95	carrier frequency fir	USPAT	WITH	ON	2006/01/30 08:33
L6	4	carrier frequency fir high	USPAT	WITH	ON	2006/01/30 08:36
L7	12	carrier frequency finite high	USPAT	WITH	ON	2006/01/30 08:38
L8	45	carrier finite high	USPAT	WITH	ON	2006/01/30 08:39
L9	9	carrier fir high	USPAT	WITH	ON	2006/01/30 08:41
L10	14	carrier fir dac	USPAT	WITH	ON	2006/01/30 08:44
L11	356	carrier dac	USPAT	WITH	ON	2006/01/30 08:44
L12	143	carrier frequency dac	USPAT	WITH	ON	2006/01/30 08:45
L13	19	carrier frequency filter dac	USPAT	WITH	ON	2006/01/30 09:27
L14	1	"4626803".pn. "30d"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 13:12
L15	1	"4626803".pn. high	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 09:28

L16	1	"5008674".pn. and fir	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:03
L17	2	"5008674".pn. and converter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:06
L18	2	"5008674".pn. and bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:19
L19	1	"5008674".pn. and time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:20
L20	2	"5008674".pn. and delay	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:24
L21	1	"5008674".pn. and pulse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:27
L22	1	"5008674".pn. and pulse WITH converter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:29
L23	1	"5008674".pn. and pulse same converter SAME filter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:30

L24	0	"5008674".pn. and broadband	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:30
L25	0	"4626803".pn. broadband	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/30 10:31
L26	2095	(341/126,144,150,152,153).CCLS.	USPAT	OR	OFF	2006/01/30 13:13
L27	2142	(375/229,230,343,350).CCLS.	USPAT	OR	OFF	2006/01/30 13:14
L28	0	(370/72,123).CCLS.	USPAT	OR	OFF	2006/01/30 13:14
L29	807	(331/32,36R,36C).CCLS.	USPAT	OR	OFF	2006/01/30 13:14

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"5323157".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/27 07:51
L2	42	delay (d ADJ1 a or dac or digital ADJ1 analog) (high or hf) (fir or response)and carrier	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/01/27 15:15
L3	5	delay (d ADJ1 a or dac or digital ADJ1 analog) (high or hf) (fir )and carrier	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/01/27 10:02
L4	2	delay (d ADJ1 a or dac or digital ADJ1 analog) (high or hf) (fir ) carrier	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/01/27 08:13
L5	30	delay (d ADJ1 a or dac or digital ADJ1 analog) (high or hf) (fir )	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/01/27 09:07
L6	14	"5521946"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/27 09:15
L7	1	"5521946" and l5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/27 09:17
L8	8	delay (d ADJ1 a or dac or digital ADJ1 analog) (high or hf) (fir )and carrier "l14"	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/27 09:16
L9	0	"5521946".pn. carrier	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/01/27 09:17